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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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2316.1107USC1	439	676.000	T. TA	2833

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I hereby certify that this paper or fee is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Assistant Commissioner for Patents, Washington, D.C. 20231.

By Linda McCormick
Name Linda McCormick

CONTINUATION APPLICATION UNDER 37 C.F.R. § 1.53(b)

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

This is a request for filing a continuation application under 37 CFR § 1.53(b) of Serial No. 09/378,105, filed on August 20, 1999 entitled JACK INCLUDING CROSSTALK COMPENSATION FOR PRINTED CIRCUIT BOARD by the following inventor(s):

Full Name Of Inventor	**Family Name** PHOMMACHANH	**First Given Name** CHANSY	**Second Given Name**
Residence & Citizenship	**City** SHAKOPEE	**State or Foreign Country** MINNESOTA	**Country of Citizenship** USA
Post Office Address	**Post Office Address** 1224 EAST SHAKOPEE, APARTMENT 132	**City** SHAKOPEE	**State & Zip Code/Country** MINNESOTA 55379/USA

1. ☒ Enclosed is a copy of the prior application; including the specification, claims, drawings, oath or declaration showing the applicant's signature, and any amendments referred to in the oath or declaration filed to complete the prior application. (It is noted that no amendments referred to in the oath or declaration filed to complete the prior application introduced new matter therein.) The continuing application is as follows: 12 pages of specification, 14 claims, 1 pages of abstract, 6 sheets of drawings, and 4 pages of oath or declaration.

☒ The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

2. ☒ Cancel original claims 2-14 of this application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

3. ☒ The filing fee is calculated below:

CLAIMS AS FILED

NUMBER FILED	NUMBER EXTRA		RATE	FEE
TOTAL CLAIMS: 1 -20	0	x	$18.00	0.00
INDEPENDENT CLAIMS 1 -3	0	x	$78.00	0.00
			BASIC FILING FEE:	$690.00
			TOTAL FILING FEE:	690.00

☐ A Verified Statement that this filing is by a small entity is already filed in the prior application.

☐ A Verified Statement that this filing is by a small entity is attached.

4. ☒ Payment of fees:
   ☒ Attached is a check in the amount of 690.00.
   ☐ Please charge Deposit Account No. 13-2725.

5. ☒ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 CFR §§ 1.16 to 1.18 which may be required by this paper or credit any overpayment to Account No. 13-2725.

6. ☒ Amend the specification by inserting before the first line the sentence:

   "This application is a continuation of application Serial No. 09/378,105, filed August 20, 1999, which application(s) are incorporated herein by reference."

7. ☒ A set of formal drawings (7 sheets) is enclosed.

8. ☐ Priority of application Serial No. , filed on in , is claimed under 35 U.S.C. 119.

   ☐ The certified copy has been filed in prior application Serial No. 09/378,105, filed August 20, 1999.

9. ☒ The prior application is assigned of record to ADC Telecommunications, Inc. located at Minnetonka, Minnesota.

10. ☒ The Power of Attorney in the prior application is to:

    Merchant & Gould P.C.
    Minneapolis, MN 55402-4131

11. ☒ A preliminary amendment will follow at a later date. (Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

    ☐ Fee for excess claims is attached.

12. ☐ A petition and fee has been filed to extend the term in the prior application until . A copy of the petition for extension of time in the prior application is attached.

13. ☐ The inventor(s) in this application are less than those named in the prior application and it is requested that the following inventors identified above for the prior application be deleted:

14. ☐ Also Enclosed:

15. ☒ Address all future communications to the **Attention of Min S. Xu** (may only be completed by attorney or agent of record) at the address below.

16. ☒ A return postcard is enclosed.

Respectfully submitted,

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Date: June 6, 2000

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Attorney Docket No. 2316.1107US01

JACK INCLUDING CROSSTALK COMPENSATION FOR PRINTED CIRCUIT BOARD

Field of the Invention

The present invention relates to electrical connectors, and specifically to electrical connectors having closely spaced contacts and printed circuit boards where interference from crosstalk in the connector is a concern.

Background of the Invention

Various electrical connectors are known for use in the telecommunications industry to transmit voice, data, and video signals. It is common for some electrical connectors to be configured to include a plug which is connectable to a jack mounted in the wall, or as part of a panel or other telecommunications equipment mounted to a rack or cabinet. The jack includes a housing which holds a plurality of closely spaced contact springs in the appropriate position for contacting the contacts of a plug inserted into the jack. The contact springs of the jack are often mounted to a printed circuit board, either vertically or horizontally. An RJ45 plug and jack connector system is one well known standard including closely spaced contacts.

Crosstalk between the contacts and circuit pathways in telecommunications connectors is a concern. U.S. Patent Nos. 5,299,956 and 5,700,167 are examples of various connectors including jacks and plugs which attempt to address the problem of crosstalk in the circuit board. It is desired to improve performance of the electrical connectors, such as an RJ45 connector, where crosstalk problems increase as higher frequencies are transmitted through the connector.

Most of the crosstalk problems occurring in a connector, such as an RJ45 connector, is mainly caused by the plug. This crosstalk is produced by the non-periodic or random discharges of crosstalk energy due to the imbalanced capacitance and/or inductance in the plug and the contact springs of a jack. RJ45 types of connectors are mainly used with balanced twisted pairs of conductors or wires. There is no grounding to shield the crosstalk energy.

One of the known techniques commonly used to solve the crosstalk problem in a connector is to balance the capacitance on the printed circuit board or on a substrate of the connector to minimize or eliminate the leaking energies from the unbalanced capacitance. The known method of reducing crosstalk generally includes forming of a capacitor by using two parallel conductive lines or wires and inducing electro-magnetic field to compensate the lesser field produced by the capacitive imbalance in the plug. This method is often referred to as capacitance balancing or capacitive compensation. The known compensation technique is applied at the nearest unbalanced components, which are the contact springs of a jack and the mated RJ45 plug. This technique is very useful for the TIA/EIA category 5 and Enhanced category 5 (5E) connector. However, the crosstalk performance of these connectors is rated only up to 100 MHz. Higher frequencies are in demand in the telecommunication and data transmission industry. The TIA/EIA category 6 connector standards have been proposed to meet the demand. Under the proposed category 6 standards, the connector is required to meet the crosstalk specifications up to 250 MHz, which is about 150% more bandwidth than the category 5's.

In order to meet this specifications, additional compensations or additional parallel conductive lines are needed to be placed on the circuit board at the nearest unbalanced components. It has been found that capacitive compensation only worsens the directivity or equal-level of the far-end crosstalk (FEXT) of the connector because the capacitor formed by two conductive lines has an inductive effect which is not accountable for. Also, it has been found that the additional compensation has a reverse capacitive effect on the near-end crosstalk (NEXT) of the connector. Generally, the far end and the near end are defined according to the two ends of the printed circuit board. The end to which signals are being injected is the near end. The opposite is the far end.

In addition, the natural crosstalk characteristic for short transmission lines, i.e. -20 dB per frequency decade, will be lost if the connector is heavily compensated. This natural crosstalk characteristic is generally required to be maintained in order for a connector to meet the category 6 crosstalk specifications.

Accordingly, the known compensation technique is either insufficient to compensate the crosstalk, or problematic by overcompensating for the crosstalk. The

known compensation technique has been considered ineffective when applied to the development of a category 6 or a category 6 type of connector, and particularly, it is unable to meet the crosstalk specifications up to 250 MHz.

Thus, there is a need for a connector including an improved crosstalk compensation technique for a printed circuit board. Further, there is a need for a connector with balanced capacitance and/or inductance on the printed circuit board to minimize or eliminate crosstalk in the connector.

Summary of the Invention

The present invention provides a method of compensating crosstalk for a printed circuit board of a connector. The present invention also provides a connector including such crosstalk compensation method.

The present method of compensating crosstalk for a printed circuit board includes a forward compensation process and a reverse compensation process. The forward compensation process compensates capacitively for the unbalanced capacitance in the plug by forming capacitors, for example, using the parallel conductive lines or wires on the printed circuit board. The reverse compensation process can be used to compensate the unbalanced capacitance and inductance caused by the forward compensations in the same pair combination of the connector. In other words, the reverse compensation negates the forward compensation at the far-end of the printed circuit board by forming capacitors, for example, using the parallel conductive lines or wires, at the far-end of the printed circuit board.

In one aspect of the present invention, the method of compensating crosstalk in a connector arrangement includes: providing a plurality of pairs of conductors on a printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel to control the transmission line impedence; sending electrical signals between the front and rear terminals; generating forward-compensating capacitance, induced between two of the pairs of conductors, proximate the respective front terminals by providing a first capacitor between a first conductor of the first pair and a second conductor of the second pair and providing a second capacitor between a second conductor of the first

pair and a first conductor of the second pair; and generating reverse–compensating capacitance/inductance to compensate the unbalanced capacitance/inductance induced between the two pairs of conductors by the first and second capacitors at the front terminal. The reverse–compensating capacitance/inductance is disposed proximate the rear terminals by providing a third capacitor between the first conductor of the first pair and the first conductor of the second pair and providing a fourth capacitor between the second conductor of the first pair and the second conductor of the second pair.

Accordingly, unbalanced capacitance/inductance, induced between the two pairs of conductors on the printed circuit board is compensated by the first, second, third, and fourth capacitors.

In one aspect of the present invention, the capacitance/inductance of the same two pairs of conductors is compensated at the opposite terminals in the reverse compensation process.

In another aspect of the present invention, the forward–reverse compensation technique can also be applied to minimize or eliminate crosstalk induced between any other combinations of two pairs of conductors on the printed circuit board.

One of the advantages of the forward–reverse compensation technique is that by reversing the compensations of ones at the opposite terminals, both the far–end crosstalk performance and the near–end crosstalk performance are improved. The inductance effect resulted from forming the capacitors at the front terminals of the printed circuit board of the connector is also balanced.

These and various other features as well as advantages that characterize the present invention will be apparent upon reading of the following detailed description and review of the associated drawings.

Brief Description of the Drawings

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several aspects of the invention and together with the description, serve to explain the principles of the invention. A brief description of the drawings is as follows:

FIG. 1 is a perspective view of a printed circuit board of one embodiment of the present invention for a telecommunications jack including contact springs at a front portion, and cable terminals at a rear portion;

FIG. 2 is a front end view of a modular jack including the circuit board of FIG. 1;

FIG. 3 is a cross-sectional side view of the jack of FIG. 2, and showing a plug mounted in the opening of the jack;

FIG. 4 is an exploded side view of the jack of FIG. 2;

FIG. 5 is a top view of the circuit board of FIG. 1, with four layers, and showing certain circuit pathways of the four layers of the illustrated preferred embodiment, including the main signal pathways between the front portion and the rear portion of the board, and additional compensation circuit pathways;

FIG. 6 is a top view of the first layer of the circuit board of FIG. 5;

FIG. 7 is a top view of the second layer of the circuit board of FIG. 5;

FIG. 8 is a top view of the third layer of the circuit board of FIG. 5;

FIG. 9 is a top view of the fourth layer of the circuit board of FIG. 5;

FIG. 10 is a more complete top view of the circuit board of FIG. 5 showing more of the circuit pathways in the preferred embodiment;

FIG. 11 is a top view of the first layer of the circuit board of FIG. 10;

FIG. 12 is a top view of the second layer of the circuit board of FIG. 10;

FIG. 13 is a top view of the third layer of the circuit board of FIG. 10;

FIG. 14 is a top view of the fourth layer of the circuit board of FIG. 10;

FIG. 15 is a table showing tip/ring pair connections and polarities applied to the ends or terminals of the tip/ring connections on the circuit board;

FIG. 16 is a table showing pair combinations and capacitance between the pairs of each pair combination;

FIG. 17 is an illustration of an example of pin configurations of a typical connector, for example, a RJ45 connector;

FIG. 18 is an illustration of capacitance between pairs I and II carried from the plug and compensating capacitance between pairs I and II at both front and rear terminals;

FIG. 19 is an illustration of capacitance between pairs I and II at the front terminals and compensating capacitance between pairs I and II at the rear terminals.

Detailed Description

Reference will now be made in detail to exemplary aspects of the present invention that are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

FIGS. 1–4 show an example of a jack 26 constructed in accordance with the principles of the present invention. In the example shown, jack 32 defines a modular jack construction for mounting to a wall plate, panel or other mounting structure. Jack 26 defines a port 30 for receiving a plug 32. A plurality of contact springs 34 are positioned within port 30 to engage one of a plurality of contacts 36 in the plug 32. The plug 32 includes a resilient latch 33. When the plug 36 is inserted into the port 30, the latch 33 interlocks with a front tab 35 of the jack 26 to retain the plug 32 within the port 30. To remove the plug 32, the latch 33 is depressed thereby allowing the plug 32 to be pulled from the port 30.

As shown in the illustrated preferred embodiment, the jack 26 and plug 32 is an 8 contact type (i.e., 4 twisted pair) connector arrangement. While the various aspects of the present invention are particularly useful for 8 contact modular connectors, it will be appreciated that other types of connectors could also be used.

Referring also to FIGS. 5–14, the jack 26 includes a printed circuit board 40 which includes a front portion 42, and a rear portion 44. The front portion 42 includes a plurality of front terminals 46 labeled 1–8. The contact springs 34 extend from the circuit board 40 at the front terminals 46 to engage the contacts 36 of the plug 32. The rear portion 44 of the circuit board 40 includes a plurality of rear terminals 48 labeled 1–8. The rear terminals 48 are connectable to cables such as through insulation displacement contacts (IDC) 49. Between the front and rear terminals 46, 48 on circuit board 40 are circuit lines or pathways 50. As will be described in greater detail below, additional circuit pathways 52 are provided to compensate for crosstalk.

The jack 26 includes a front jack housing 54, and a rear insert assembly 56 in the illustrated preferred embodiment. The jack housing 54 is adapted to be snap-fit into a face plate, panel, or other mounting arrangement.

The insert assembly 56 is adapted to snap fit within a back side 61 of the housing 54. The insert assembly 56 includes a connector mount 66, a plurality of insulation displacement terminals 68, a termination cap 70, the circuit board 40, and the contact springs 34 (e.g., eight contact springs) mounted on the circuit board 40. When assembled, the insulation displacement terminals 68 and the termination cap 70 mount at a top side of the connector mount 66, while the circuit board 40 mounts to a bottom side of the connector mount 66. As so assembled, the contact springs 34 project upward between resilient locking tabs 76 (only one shown) of the connector mount 66. The locking tabs 76 are adapted to snap fit within corresponding openings 78 defined by the housing 54. Further detail relating to an exemplary housing and connector mount suitable for practicing the present invention are disclosed in U.S. Patent Application Serial No. 09/327,053, filed June 7, 1999 that is hereby incorporated by reference. Details relating to contact spring configurations suitable for use with the present invention are disclosed in U.S. Patent Application Serial No. Not Yet Assigned, which is entitled Telecommunications Connector for High Frequency Transmissions, which has been assigned Attorney Docket No. 2316.1067US01, which was filed on a date concurrent with the filing date of this application, and which is hereby incorporated by reference. Other spring configurations are possible, such as those shown in U.S. Patent Application Serial No. 09/231,736, filed January 15, 1999 hereby incorporated by reference. Other spring configurations are possible for use with circuit board 40, as desired. Further, front terminals 46 are shown in 3 rows across board 40 in the preferred embodiment. Other arrangements are possible such as more or less rows.

FIG. 3 shows the modular plug 32 inserted within the port 30 defined by a front side 84 of the housing 54. The plug 32 includes eight contacts 36 that provide electrical connections with the contact springs 34 of the modular jack 26 when the plug 32 is inserted within the port 30. For example, FIG. 3 shows one of the contacts 36 in electrical contact with one of the contact springs 34. As shown in FIGS. 1, 3 and 4, the contact springs 34 are in a deflected orientation, such as that caused by the contacts 36

of plug 32. In the undeflected orientation, contact springs 34 have their free ends further spaced from board 40 than the illustrated deflected orientation.

In FIG. 5, the circuit board 40 preferably includes four layers shown in FIGS. 6–9, respectively. Circuit pathways between front terminals 46 labeled 1–8 at the front portion 42 and rear terminals 48 labeled 1–8 at the rear portion 44 are all shown in FIG. 5 for explanation purposes. FIGS. 6–9 illustrate a preferred layout of the circuit pathways in four layers, such that the crossover between the conductive lines or wires is on different layers. The illustrated layout of the pathways conforms with the industry standards. The front terminal or pin 46–1 is connected to the opposite rear terminal or pin 48–1 via a transmission path or conductor 50–1. Similarly, the other front terminals or pins 46–N are connected to the rear terminals or pins 48–N, respectively, via transmission paths 50–N.

In a typical terminal pin assignments, such as in a RJ45 connector, best shown in FIG. 15, transmission paths 50–4 and 50–5 form a pair I where transmission path 50–5 is a tip line, and transmission path 50–4 is a ring line; transmission path 50–3 and 50–6 form a pair II where transmission path 50–3 is a tip line, and transmission path 50–6 is a ring line; transmission paths 50–1 and 50–2 form a pair III where transmission path 50–1 is a tip line, and transmission path 50–2 is a ring line; and transmission paths 50–7 and 50–8 form a pair IV where transmission path 50–7 is a ring line, and transmission path 50–8 is a ring line. The tip terminal generally has a positive polarity, and the ring terminal generally has a negative polarity. It is appreciated that the pin assignments can be varied without departing from the principles of the present application. For example, transmission path 50–3 and 50–6 can be referred to as pair III, and transmission path 50–1 and 50–2 can be referred to as pair II.

In FIG. 5, the transmission paths of each pair are substantially parallel to each other. As shown, the transmission paths 50–4 and 50–5 are parallel; the transmission paths 50–3 and 50–6 are parallel; the transmission paths 50–1 and 50–2 are parallel; the transmission paths 50–7 and 50–8 are parallel. These are the main signal pathways between the front portion 42 and the rear portion 44 of the circuit board 40.

In addition, in FIG. 5, compensation conductive lines 52 are added and disposed in parallel to form capacitors 52–C. The added capacitors compensate the

unbalanced capacitance carried from the plug to the front portion 42 of the circuit board 40. In FIG. 16, a table of capacitance between each two pairs of transmission paths are shown. By way of an example, between pairs I and II, there are four capacitance, C34, C35, C65, C64. As illustrated in FIG. 17, due to the distance and/or location of the contacts in the plug, C34 is larger than C35, and C65 is larger than C64. Thus, the capacitance is unbalanced between C34 and C35 in the I/II pairs. Also, the capacitance is unbalanced between C65 and C64 in the I/II pairs.

The forward compensation is illustrated in FIG. 18. At the front portion 42 of the connector, a capacitor C35' is added in dashed lines between terminals 46–3 and 46–5, such that the capacitance between terminals 46–3 and 46–4 and the capacitance between terminals 46–3 and 46–5 are balanced.

Similarly, in FIG. 18, a capacitor C64' is added in dashed lines between terminals 46–4 and 46–6, such that the capacitance between terminals 46–4 and 46–6 and the capacitance between terminals 46–5 and 46–6 are balanced.

As shown in FIG. 18, at the rear portion 44, the capacitance is generally minimal due to the isolation provided by the isolation displacement contacts (IDCs) 49 (FIG. 4). However, the addition of the capacitors C35' and C64' causes capacitance/inductance unbalance on the printed circuit board between the front and rear portions. To compensate for such induced unbalance of the capacitance on the printed circuit board, a capacitor C65' is further added in dashed lines between rear terminal 48–5 and rear terminal 48–6; and a capacitor C34' is further added in dashed lines between rear terminal 48–3 and rear terminal 48–4, as shown in FIG. 19. Accordingly, the capacitance/inductance with respect to pairs I and II between the front and rear portions of the printed circuit board is balanced. In other words, C65' and C34' reverse–compensate the capacitance/inductance unbalance caused by the addition of C35' and C64'.

As shown in FIG. 5, the forward compensation is performed at the front portion 42. The capacitor C35' between terminal 46–3 and terminal 46–5 is formed by two parallel conductive lines 52–C35'. The capacitor C64' between terminal 46–6 and terminal 46–4 is formed by two parallel conductive lines 52–C64'. Additional capacitors, such as 52–C64'' and 52–C35'', can be used if desired to increase or adjust the capacitance at the front portion 42.

Also as shown in FIG. 5, the reverse compensation is performed at the rear portion 44. The capacitor C65' between terminal 48–6 and terminal 48–5 is formed by two parallel conductive lines 52–C65'. The capacitor C34' between terminal 48–3 and terminal 48–4 is formed by two parallel conductive lines 52–C34'. It is appreciated that additional capacitors can be used if desired to balance the capacitance/inductance resulted from the front portion 42.

The compensating conductive lines 52 are terminated on the isolation displacement contacts with a preferable 100 Ohm resistor as generally specified in the industry. It is appreciated that other resistance can be used at the terminal within the scope of the present invention. Further, the shape or type of compensating capacitors can be varied. For example, C64', C35', C34', C64'', and C35'' are capacitors formed on the same layer as shown in FIGS. 6–9. As shown in FIGS. 6–7, C65' is formed on two different layers. Also, as shown in FIG. 8, C35'' is formed between transmission path 50–3 and an additional compensating conductive line 52–5. It is appreciated that other forms of an electro–magnetic field besides capacitors can be used within the scope of the present invention.

In a preferred printed circuit board arrangement, the layer shown in FIG. 6 is the first layer of the circuit board 40, the layer shown in FIG. 7 is the second layer of the circuit board 40, the layer shown in FIG. 8 is the third layer of the circuit board 40, and the layer shown in FIG. 9 is the fourth layer of the circuit board 40. It is appreciated that other printed circuit board arrangements can be used without departing from the principles of the present invention.

Accordingly, by reversing the compensations of ones at opposite terminals, i.e. at the rear portion 44, the forward–reverse compensation processes allow the capacitance/inductance induced between pair I and pair II to be balanced on the printed circuit board. As a result, crosstalk caused by the imbalanced capacitance/inductance of pair I and pair II is minimized or eliminated.

It is appreciated that the imbalance capacitance/inductance caused by the other pair combinations, such as the other five pair combinations shown in FIG. 16, i.e., I III, I IV, II/III, II/IV, and III/IV, can be minimized or eliminated by applying the same principle of the present invention. It is also noted that the imbalance

capacitance/inductance caused by pairs III/IV may be negligible due to the far distance between the two pairs.

FIG. 10 illustrates a top view of a more complete capacitance/inductance compensation arrangement on the printed circuit board 40 in a preferred embodiment. It is more complete in a sense that capacitance/inductance imbalance from the other pair combinations (except the combination of pair III and pair IV) are considered. Accordingly, additional capacitors, such as 52–C13', can be used to minimize or eliminate the capacitance imbalance induced by pair II and pair III. In FIG. 11, the capacitor C13' is formed by a conductive line 52–C13' between the terminal 46–1 and the terminal 46–3. In each case, once a capacitor is added to compensate the capacitance imbalance at the front portion 42, another capacitor, for example, 52–C23', is added to compensate the capacitance/inductance imbalance at the rear portion 44. The capacitors for pair combinations (except pair combination III/IV) are 52–C46', 52–C68', 52–C25', 52–C65', 52–C67', and 52–C67" as shown in FIG. 11; 52–C68", 52–C58', 52–C13", 52–C53', 52–C57', 52–C23', and 52–C15' as shown in FIG. 12; 52–C47', 52–C35', and 52–C34'as shown in FIG. 13; 52–C46", 52–C14', and 52–C26' as shown in FIG. 14. It is appreciated the layout of the resistors can be changed between the layers without departing the scope of the present invention. It is noted that when the space on one layer for a compensating capacitor, for example 52–C67', is not sufficient, additional compensating capacitor 52–C67" is formed in a different layer.

In a preferred embodiment, the layer shown in FIG. 11 is the first layer of the circuit board of FIG. 10. The layer shown in FIG. 12 is the second layer of the circuit board of FIG. 10. The layer shown in FIG. 13 is the third layer of the circuit board of FIG. 10. The layer shown in FIG. 14 is the fourth layer of the circuit board of FIG. 10. It is appreciated that other circuit layer arrangements in the connector can be used within the scope of the present invention.

It will be appreciated that the forward–reverse compensating technique can also be used to compensate unbalanced inductance in the plug and/or contact springs by forming additional capacitors in the reverse compensation process.

It will also be appreciated that other types of electro–magnetic field can be used to compensate unbalanced capacitance/inductance on the printed circuit board.

For example, the electro–magnetic field can be a combination of capacitor and an inductor.

It is further appreciated that the capacitors and/or inductors used in the forward–reverse compensation technique can be implemented in other parts of the connector, i.e. not necessarily on the printed circuit board, without departing from the principles of the present invention.

The forward–reverse crosstalk compensation technique of the present invention significantly improves the near–end as well as the far–end crosstalk performance. For example, the near–end crosstalk can be as low as −64 dB at 100 MHz frequency and as low as −48 at 250 MHz frequency. The far–end crosstalk can be as low as −52 dB at 100 MHz frequency and as low as −44 dB at 250 MHz.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

What Is Claimed Is:

1. A method of compensating cross–talk in a connector arrangement, comprising:

providing a plurality of pairs of conductors on a printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel;

sending electrical signals between the front and rear terminals;

generating forward–compensating capacitance, induced between two of the pairs of conductors, proximate the respective front terminals by providing a first capacitor between a first conductor of the first pair and a second conductor of the second pair and providing a second capacitor between a second conductor of the first pair and a first conductor of the second pair;

generating reverse–compensating capacitance/inductance, induced between the two pairs of conductors and caused by the first and second capacitors at the front terminal, proximate the respective rear terminals by providing a third capacitor between the first conductor of the first pair and the first conductor of the second pair and providing a fourth capacitor between the second conductor of the first pair and the second conductor of the second pair; and

wherein unbalanced capacitance/inductance, induced between the two pairs of conductors on the printed circuit board is compensated by the first, second, third, and fourth capacitors.

2. A connector arrangement for compensating cross–talk comprising:

a printed circuit board with front and rear terminals;

a plurality of pairs of conductors on the printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel;

a forward–compensating capacitance inducing capacitance between two of the pairs of conductors, proximate the respective front terminals, the forward–compensating capacitance including a first capacitor between a first conductor of the first pair and a second conductor of the second pair, and a second capacitor between a second conductor of the first pair and a first conductor of the second pair;

a reverse–compensating capacitance inducing capacitance/inductance between the two pairs of conductors, proximate the respective rear terminals, the reverse–compensating capacitance including a third capacitor between the first conductor of the first pair and the first conductor of the second pair, and a fourth capacitor between the second conductor of the first pair and the second conductor of the second pair; and

wherein unbalanced capacitance/inductance, induced between the two pairs of conductors on the printed circuit board is compensated by the first, second, third, and fourth capacitors.

3. The connector arrangement of claim 2, wherein the front terminals include contact springs.

4. The connector arrangement of claim 2, wherein the rear terminals include insulation displacement connectors.

5. The connector arrangement of claim 3, further comprising a housing holding the printed circuit board, the housing defining a plug port for receipt of a plug of a telecommunications cable.

6. The connector arrangement of claim 2, further comprising a housing holding the printed circuit board, the housing defining a plug port for receipt of a plug of a telecommunications cable.

7. A cross–talk compensating member for use in a connector arrangement in a communication system, comprising:

(a) a planar substrate;

(b) front terminal members on said substrate for conductively receiving the first and second leads of at least two conductor pairs;

(c) rear terminal members on said substrate;

(d) a conductive main pathway on said substrate between each one of said front terminal members and one of said rear terminal members;

(e) said front terminal members, conductive main pathways and rear terminal members cooperating to form at least two pairs of signal pathways through said cross–talk compensating member;

(f) a first pair of parallel conductive compensating pathways on said substrate, each compensating pathway of said first pair connected to one front terminal member from each pair of signal pathways to define a first capacitor;

(g) a second pair of parallel conductive compensating pathways on said substrate, each compensating pathway of said second pair connected to a rear terminal member from each pair of signal pathways to define a second capacitor, one of the rear terminal members of said second capacitor being part of a different signal pathway than one of said front terminal members of said first capacitor.

8. The connector arrangement of claim 7, wherein the front terminal members include contact springs.

9. The connector arrangement of claim 7, wherein the rear terminal members include insulation displacement connectors.

10. A cross–talk compensating member for use in a connector arrangement in a telecommunication system, comprising:

(a) a planar substrate;

(b) front terminal members (1–8) on said substrate for conductively receiving four conductor pairs of first and second leads of a connector plug;

(c) rear terminal members (1–8) on said substrate;

(d) a conductive main pathway (1–8) on said substrate between each one of said front terminal members (1–8) with one of said rear terminal members (1–8);

(e) said front terminal members (1–8), conductive main pathways (1–8) and rear terminal members cooperating to form pairs of signal pathways (1–2, 3–6, 4–5, 7–8) through said cross–talk compensating member;

(f) two first pairs of parallel conductive compensation pathways on said substrate, one of the first pairs of parallel conductive compensation pathways extending from the front terminal member (3) and (5), the other of the first pair of parallel conductive compensation pathways extending from the front terminal members (4) and

(6), each of the first pairs of parallel conductive compensation pathways defining a capacitor;

(g) two second pairs of parallel conductive compensation pathways on said substrate, one of the second pairs of parallel conductive compensation pathways extending from the rear terminal members (3) and (4), the other of the second pair of parallel conductive compensation pathways extending from the rear terminal members (5) and (6), each of the second pairs of parallel conductive compensation pathways defining a capacitor.

11. The connector arrangement of claim 10, wherein the front terminal members include contact springs.

12. The connector arrangement of claim 10, wherein the rear terminal members include insulation displacement connectors.

13. A method of compensating cross–talk in a connector arrangement, comprising:

providing a plurality of pairs of conductors on a printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel;

sending electrical signals between the front and rear terminals;

generating forward–compensating capacitance, induced between two of the pairs of conductors, proximate the respective front terminals by providing a first electro–magnetic field between a first conductor of the first pair and a second conductor of the second pair and providing a second electro–magnetic field between a second conductor of the first pair and a first conductor of the second pair;

generating reverse–compensating capacitance/inductance, induced between the two pairs of conductors and caused by the first and second capacitors at the front terminal, proximate the respective rear terminals by providing a third electro–magnetic field between the first conductor of the first pair and the first conductor of the second pair and providing a fourth electro–magnetic field between the second conductor of the first pair and the second conductor of the second pair; and

wherein unbalanced capacitance/inductance, induced between the two pairs of conductors on the printed circuit board is compensated by the first, second, third, and fourth electro–magnetic fields.

14. A connector arrangement for compensating cross–talk comprising:

a printed circuit board with front and rear terminals;

a plurality of pairs of conductors on the printed circuit board, the pairs of conductors connecting to respective front and rear terminals, each pair of conductors including a ring conductor and a tip conductor, and the ring and tip conductors being substantially disposed in parallel;

a forward–compensating capacitance inducing capacitance between two of the pairs of conductors, proximate the respective front terminals, the forward–compensating capacitance including a first electro–magnetic field between a first conductor of the first pair and a second conductor of the second pair, and a second electro–magnetic field between a second conductor of the first pair and a first conductor of the second pair;

a reverse–compensating capacitance/inductance inducing capacitance/inductance between the two pairs of conductors, proximate the respective rear terminals, the reverse–compensating capacitance/inductance including a third electro–magnetic field between the first conductor of the first pair and the first conductor of the second pair, and a fourth electro–magnetic field between the second conductor of the first pair and the second conductor of the second pair; and

wherein unbalanced capacitance/inductance, induced between the two pairs of conductors on the printed circuit board is compensated by the first, second, third, and fourth electro–magnetic fields.

Abstract of the Disclosure

A forward-reverse crosstalk compensation method is provided for compensating capacitance/inductance on a printed circuit board of a connector. The method includes a forward compensation process and a reverse compensation process. The forward compensation process compensates the unbalanced capacitance in the plug of the connector by using the parallel conductive lines or wires. The reverse compensation process can be used to compensate the unbalance capacitance/inductance caused by the forward compensations in the same pair combination of the connector. In both forward compensation and reverse compensation processes, electro-magnetic fields, such as capacitors, can be formed to balance the capacitance/inductance on the printed circuit board of the connector.

FIG. 1

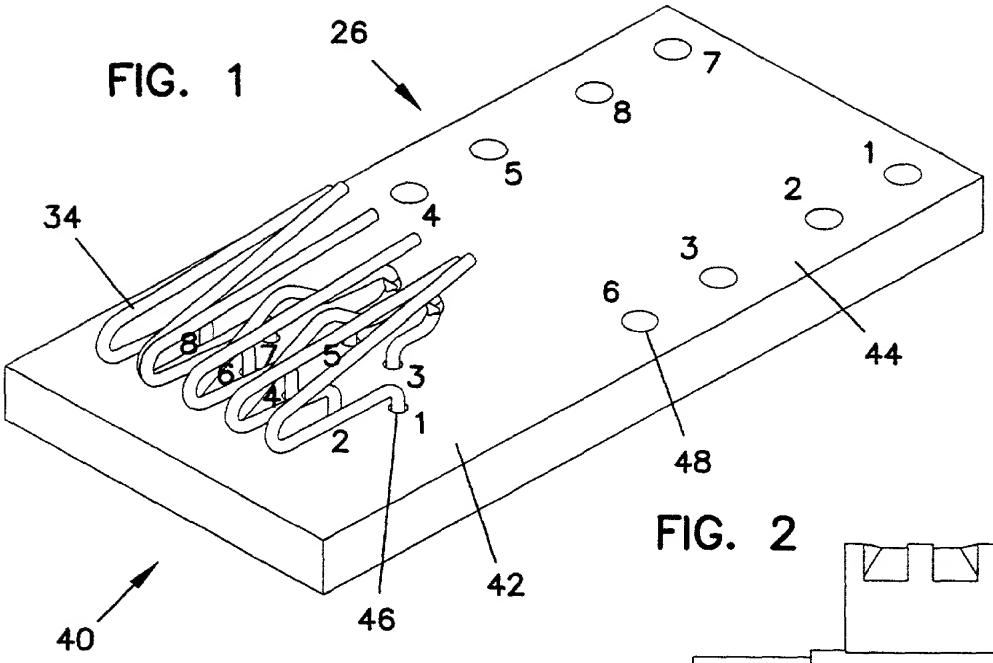


FIG. 2

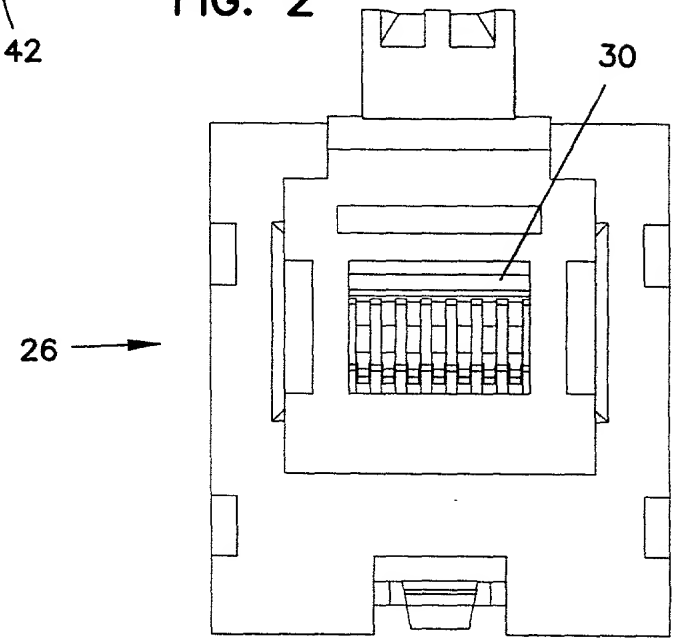


FIG. 3

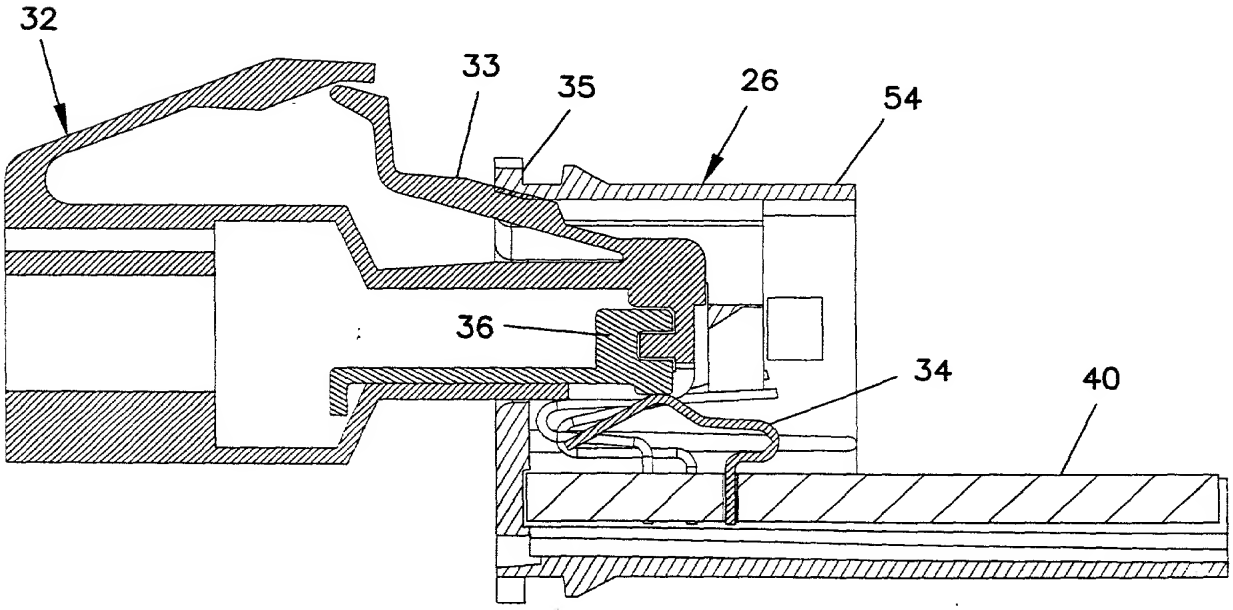


FIG. 4

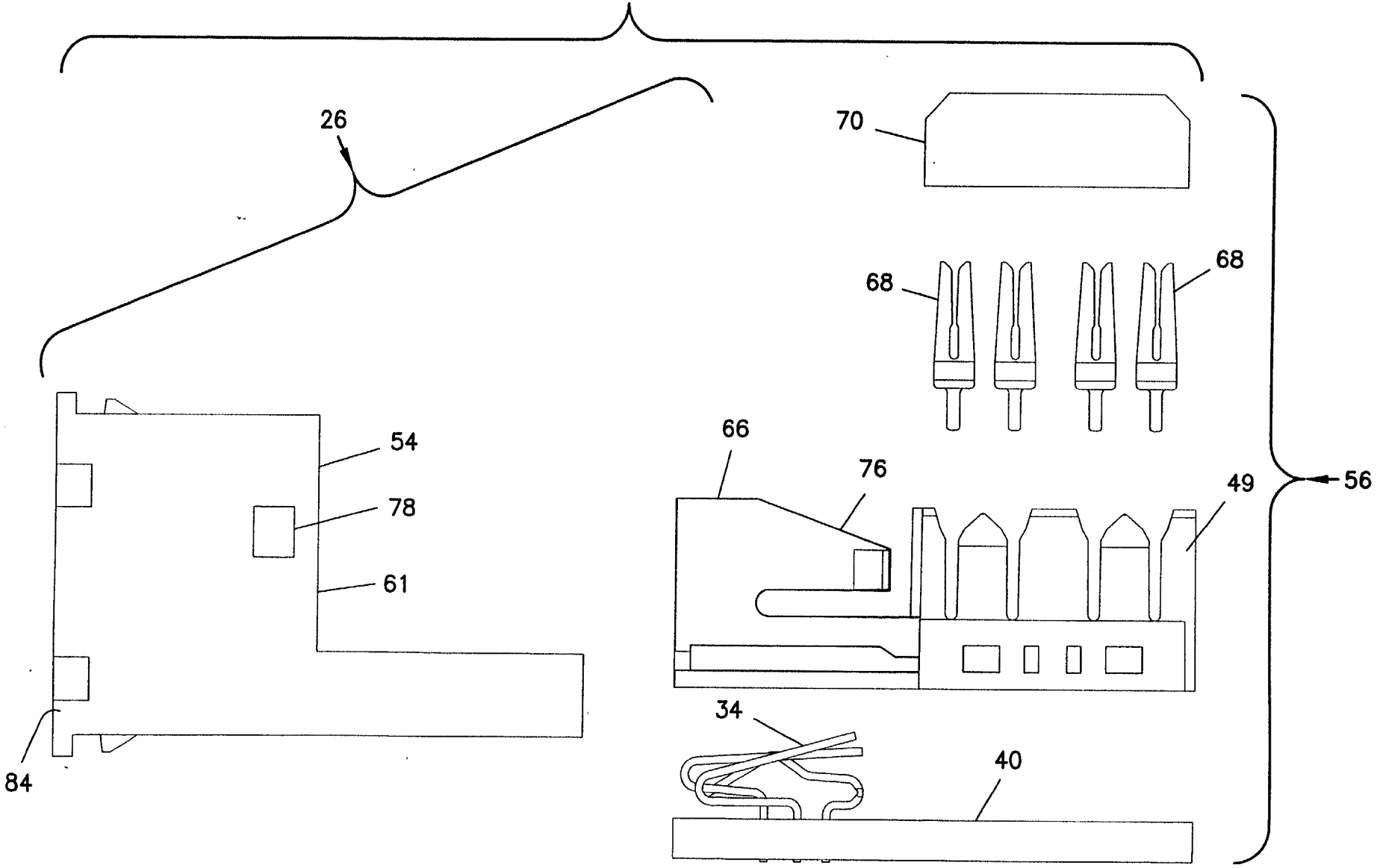


FIG. 5

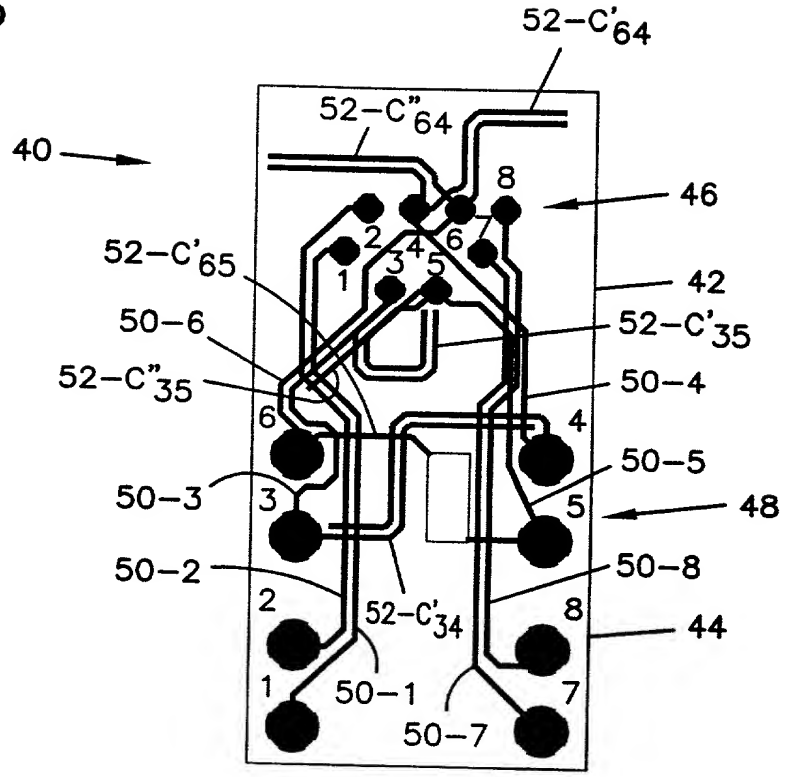
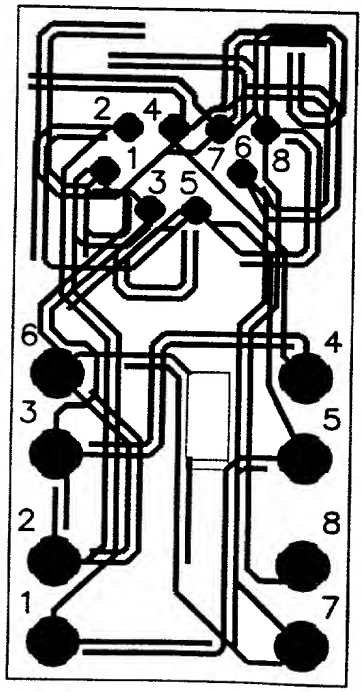

52–C'64
52–C"64
40
8
46
2
4
6
52–C'65
1
3
5
42
50–6
52–C'35
52–C"35
50–4
6
4
50–5
50–3
3
5
48
50–2
50–8
2
52–C'34
8
44
1
50–1
7
50–7

FIG. 10


2
4
1
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6
8
3
5
6
4
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1
7

FIG. 6

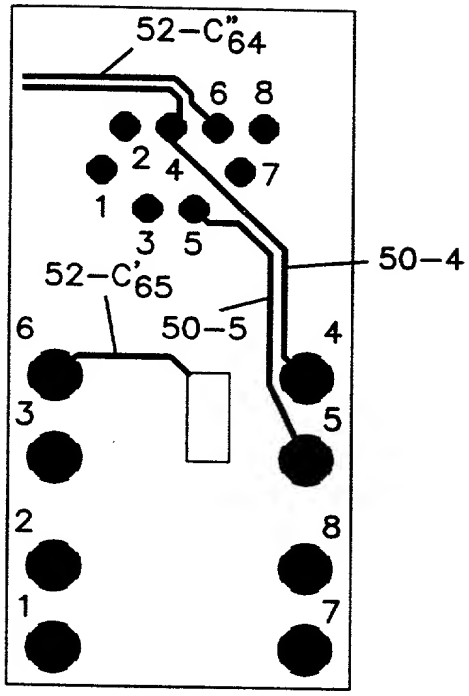


FIG. 7

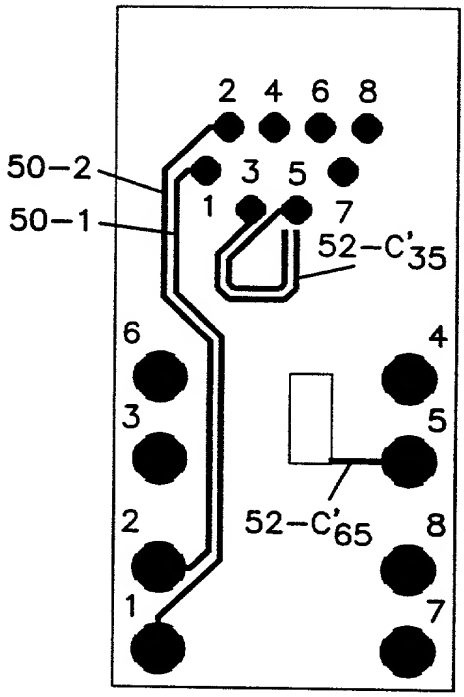


FIG. 8

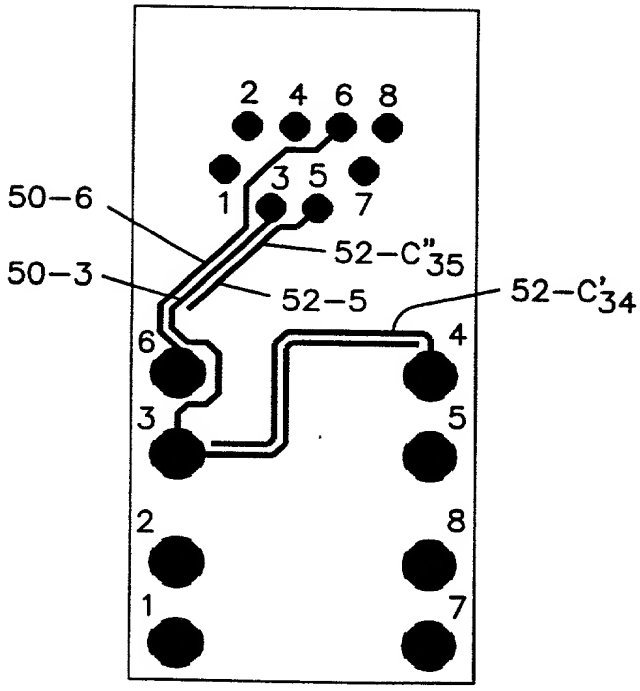


FIG. 9

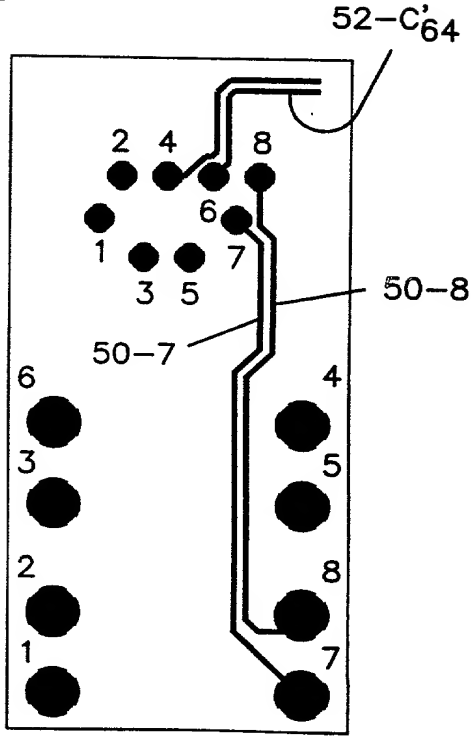


FIG. 11

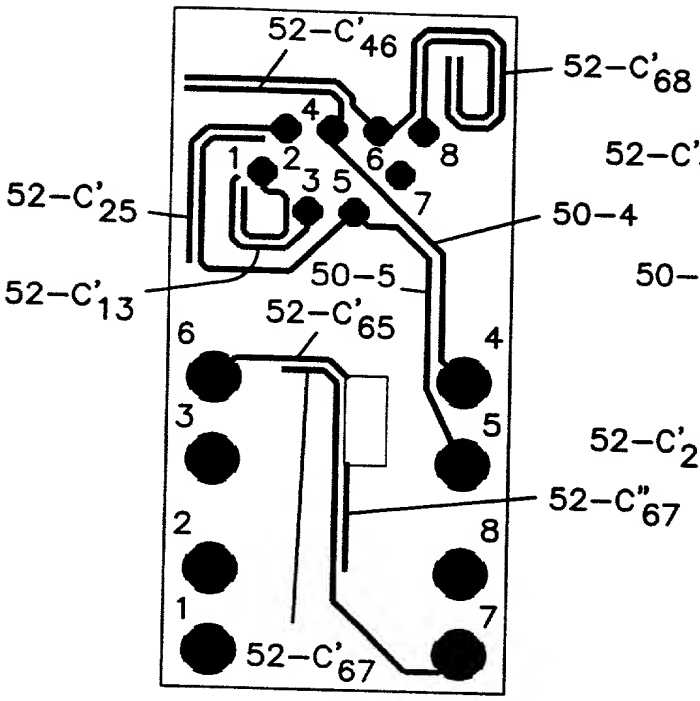


FIG. 12

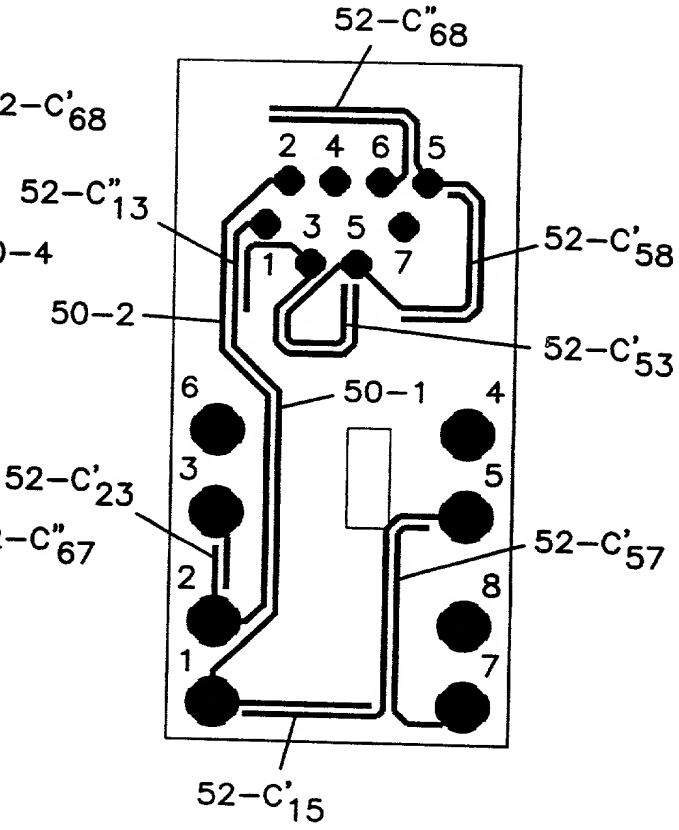


FIG. 13

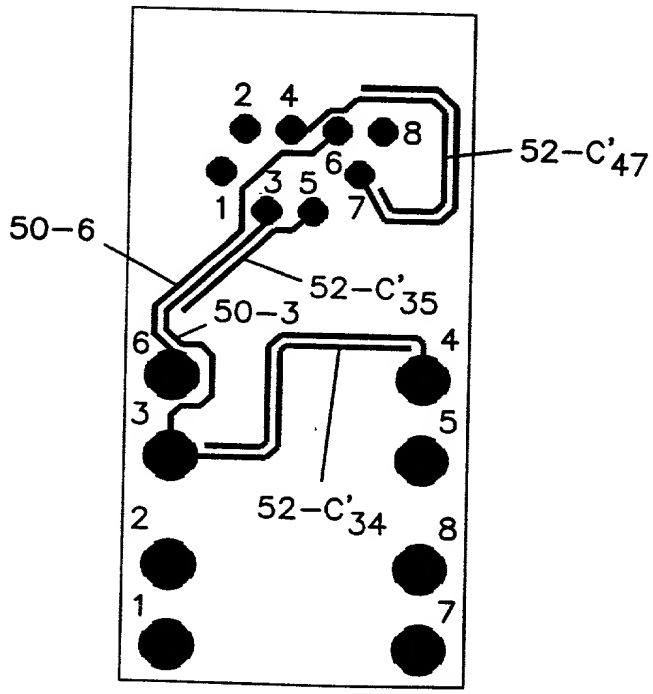


FIG. 14

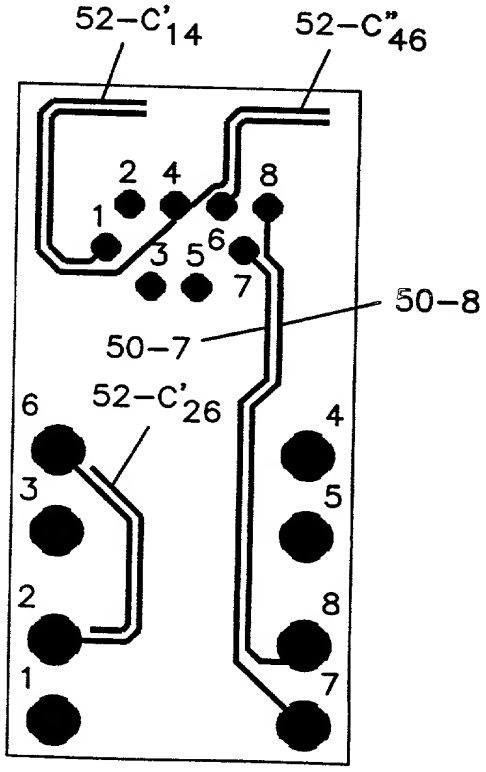


FIG. 15

PAIR	PIN TERMINALS	TIP/RING	POLARITY
I	5 4	T R	+ −
II	3 6	T R	+ −
III	1 2	T R	+ −
IV	7 8	T R	+ −

FIG. 16

PAIR COMBINATIONS	CAPACITANCE BETWEEN PAIRS
I/II	C34, C35, C65, C64
I/III	C14, C15, C24, C25
I/IV	C47, C48, C57, C58
II/III	C13, C16, C23, C26
II/IV	C37, C38, C67, C68
III/IV	C17, C18, C27, C28

FIG. 17

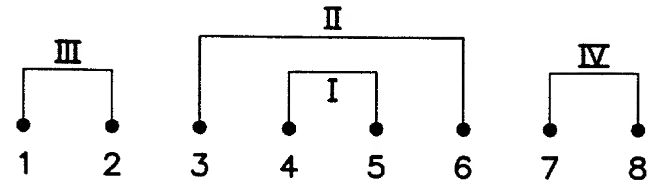


FIG. 18

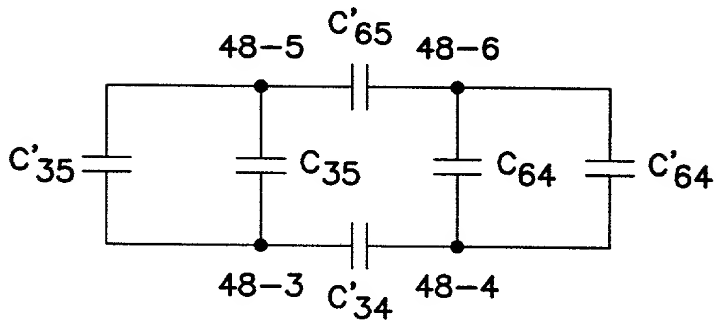
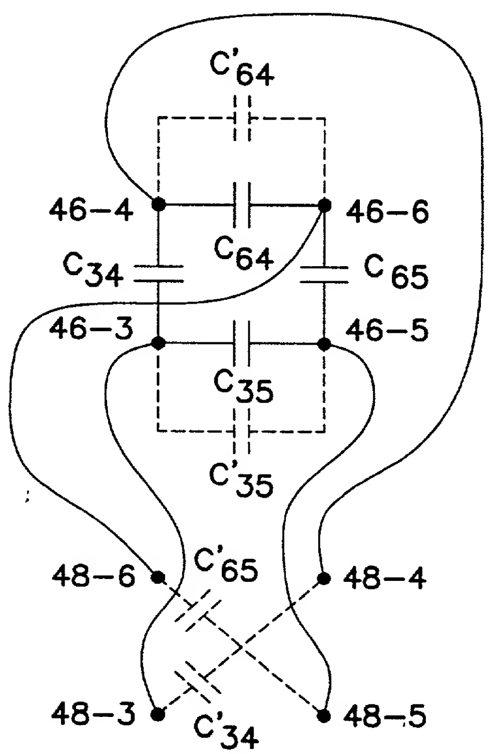


FIG. 19



Attorney Docket No. 2316.1107US01

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **JACK INCLUDING CROSSTALK COMPENSATION FOR PRINTED CIRCUIT BOARD**

The specification of which
a. ☐ is attached hereto
b. ☒ was filed on August 20, 1999 as Attorney Docket No. 2316.1107US01 and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed and as amended on (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)

I hereby appoint the following attorney(s) /or patent agent(s) to prosecute this applicatio d to transact all business in the Patent and Trademark Office connected herewith:

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Anderson, Gregg I.	Reg. No. 28,828	Larson, James A.	Reg. No. 40,443
Ansems, Gregory M.	Reg. No. 42,264	Liepa, Mara E.	Reg. No. 40,066
Batzli, Brian H.	Reg. No. 32,960	Lindquist, Timothy A.	Reg. No. 40,701
Beard, John L.	Reg. No. 27,612	McDonald, Daniel W.	Reg. No. 32,044
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Epp Ryan, Sandra	Reg. No. 39,667	Storer, Shelley D.	Reg. No. P-45,135
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Goggin, Matthew J.	Reg. No. 44,125	Sumners, John S.	Reg. No. 24,216
Golla, Charles E.	Reg. No. 26,896	Swenson, Erik G.	Reg. No. P-45,147
Gorman, Alan G.	Reg. No. 38,472	Tellekson, David K.	Reg. No. 32,314
Gould, John D.	Reg. No. 18,223	Trembath, Jon R.	Reg. No. 38,344
Gregson, Richard	Reg. No. 41,804	Underhill, Albert L.	Reg. No. 27,403
Gresens, John J.	Reg. No. 33,112	Vandenburgh, J. Derek	Reg. No. 32,179
Hamre, Curtis B.	Reg. No. 29,165	Welter, Paul A.	Reg. No. 20,890
Hillson, Randall A.	Reg. No. 31,838	Wahl, John R.	Reg. No. 33,044
Holzer, Jr., Richard J.	Reg. No. 42,668	Whipps, Brian	Reg. No. 43,261
Johnston, Scott W.	Reg. No. 39,721	Wickhem, J. Scot	Reg. No. 41,376
Kadievitch, Natalie D.	Reg. No. 34,196	Williams, Douglas J.	Reg. No. 27,054
Kastelic, Joseph M.	Reg. No. 37,160	Witt, Jonelle	Reg. No. 41,980
Kettelberger, Denise	Reg. No. 33,924	Xu, Min S.	Reg. No. 39,536
Knearl, Homer L.	Reg. No. 21,197	Zeuli, Anthony R.	Reg. No. P-45,255
Kowalchyk, Alan W.	Reg. No. 31,535		
Kowalchyk, Katherine M.	Reg. No. 36,848		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
3100 Norwest Center
90 South Seventh Street
Minneapolis, MN 55402-4131

I hereby declare that all statements made h .n of my own knowledge are true and that all st .ients made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	**Full Name Of Inventor**	**Family Name** PHOMMACHANH	**First Given Name** CHANSY	**Second Given Name**
0	**Residence & Citizenship**	**City** Shakopee	**State or Foreign Country** Minnesota	**Country of Citizenship** U.S.A.
1	**Post Office Address**	**Post Office Address** 1224 East Shakopee. Apartment 132	**City** Shakopee	**State & Zip Code/Country** Minnesota 55379 U.S.A.
Signature of Inventor 201: Chansy Phommachanh				**Date:** 9-5-07

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)–(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;

or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden–of–proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.